UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/853,506	05/11/2001	Mark L. Janecek	END920000132US1	6858

7590 09/18/2003

Mark Levy
Salzman & Levy
19 Chenango St., Ste. 902
Binghamton, NY 13901

EXAMINER	
ALCALA, JOSE H	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 09/18/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 0803

Application Number: 09/853,506

Filing Date: May 11,2001

Appellant(s): MARK L. JANECEK,JOHN S. KRESGE,MARK V. PIERSON,

Mark Levy
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed June 2,2003

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The amendment after final rejection filed on 3/11/03 has not been entered.

(5) Summary of Invention

The summary of invention contained in the brief is deficient because it does not refer to the specification by page or line number, or to the drawing by reference characters.

The following is a correct summary of the invention, necessary for a clear understanding of the claimed invention.

The invention features a circuit board laminate 10 comprising an inner power core 14 that is connected between two signal cores 12. Upon lamination of the cores, the circuit board structure is electrically connected. The laminated circuit board inner power core 14 comprises filled via through holes of conductive adhesive 16. The conductive power core vias 16 make contact with the metal pads 3 of the conductive vias of the respective outer signal cores 15, upon lamination.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The rejection of claims 1,2,4-7,11,12 and 14 stand or fall together because appellant's brief does not include a statement that this grouping of claims does not stand or fall together and reasons in support thereof. See 37 CFR 1.192(c)(7).

(8) Claims Appealed

A substantially correct copy of appealed claim 9 appears on page 4 of the Appendix to the appellant's brief. The minor errors are as follows: claim 9 should be labeled as cancelled, according to amendment filed on 1/10/02.

(9) Prior Art of Record

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal:

5,640,761	Di Stefano	6-1997

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1,2,4-7,11,12,14 are rejected under 35 U.S.C. 102(b) as being anticipated by DiStefano et al (US Patent No. 5,640,761).

Regarding Claim 1, DiStefano teaches a three-layered laminated circuit structure, comprising: a first substrate (top substrate of Figure 2) having conductive via through

holes (Reference number 26) disposed therein; and a second substrate (second substrate from top to bottom core of Figure 2) laminated to said first substrate and having conductive, adhesive-filled via through holes (the holes that are filled with Reference number 48) that align with, and make electrical contact with, the conductive via through holes (reference number 26) of said first substrate upon lamination of said first and second substrates, and a third substrate (third substrate from top to bottom of Figure 2) laminated to said second substrate having via through holes (reference number 26) that align with, and make electrical contact with, the adhesive filled via through holes of said second substrate, thus forming said three-layered, laminated circuit structure (see Figure 3).

Regarding Claim 2, DiStefano teaches that the first and third substrates (top substrate and the third substrate from the top of Figure 4) each comprise a signal core layer (the layer contains reference number 30), and said second substrate layer comprises a power core layer (the layer that contains reference number 42).

Regarding Claim 4, DiStefano teaches that said via through holes (the holes that are filled with Reference number 48) of said power core layer comprise undercut contact surfaces (the top and bottom surfaces of the conductive material reference number 48 inside the via through hole, as seen in Figure 3), and said via through holes of each of said signal core layers have metallic pads (pads of conductive layers with reference numbers 24 and 22 in Figure 3) that make electrical contact with said undercut contact surfaces of said via trough holes of said power core layer..

Regarding Claim 5, DiStefano teaches a multi-layered circuit structure, comprising: a first substrate (top substrate of Figure 2) having conductive via through holes (reference number 26) disposed therein; and a second substrate (second substrate from the top of Figure 4) laminated to said first substrate, and having via through holes (the hole where reference number 48 is located) comprising conductive adhesive coated pads (the pads at 56a) that align with, and make electrical contact with, the conductive via through holes (reference number 26) of said first substrate.

Regarding Claim 6, DiStefano teaches that said first substrate (top substrate of Figure 2) comprises a signal core layer (the layer contains reference number 30), and said second substrate comprises a power core layer (the layer that contains reference number 42).

Regarding Claim 7, DiStefano teaches further comprising a third substrate (the third substrate from the top of figure 2) having similar structure to that of said first substrate (See Figure 2, where both substrates are "similar"), said first and third substrates each being laminated to said second substrate (See figure 3), and wherein said first and third substrates each define a signal core layer (both layers containing reference number 30), said second substrate further defining an inner power core layer (the layer that contains reference number 42) sandwiched between each of said signal core layers (See Figures 2 and 3).

Regarding Claim 11, DiStefano teaches a multi-layered circuit structure, comprising: first (top substrate of Figure 2) and second (third substrate from the top of Figure 2) substrates, each having conductive via through holes (Reference numbers 26)

disposed therein; and a third substrate (second substrate from the top of Figure 2) laminated between said first and second substrates (See Figures 2 and 3) and having conductive adhesive filled via through holes (the holes containing reference number 48) that align with, and make electrical contact with, the conductive via through holes of said first and second substrates (See Figure 3).

Regarding Claim 12, DiStefano teaches that said first (top substrate of Figure 2) and second (third substrate from the top of Figure 2) substrates comprise a signal core layer (both layers that contain reference number 30), and said third substrate comprises a power core layer (the layer that contains reference number 42).

Regarding Claim 14, DiStefano teaches that said via through holes (the holes that are filled with Reference number 48) of said inner power core layer comprise undercut contact surfaces (the top and bottom surfaces of the conductive material reference number 48 inside the via through hole, as seen in Figure 3), and said via through holes of each of said signal core layers have metallic pads (the pads of the thorough holes with reference numbers 26) that make electrical contact with said undercut contact surfaces of said via trough holes of said power core layer (See Figures 3 and 4).

(11) Response to Argument

Appellant argues, on page 5 of the Appeal Brief, that: *"the interposer or second layer 12 is not designed as a power core layer"*. However, the examiner respectfully disagrees with this argument. DiStefano teaches an intermediate layer (second

substrate from the top of Figure 2), laminated between two layers (first and third substrates from the top in Figure 2). The layer of DiStefano is reasonably construed as a power core, because the layer has a conductive member inside (reference number 48), which is a mean of supplying energy. Furthermore, this layer is structurally identical to applicant's power core layer, which is: "laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate". Therefore, we can conclude that the interposer or second layer (second substrate from the top of Figure 2) is a power core layer.

Appellant further argues, on page 5 of the Appeal Brief, that: *"Neither does this layer have a distinct plated via through hole that aligns with plated via through holes of the first and second layers"*. In response to applicant's argument, it is noted that the features upon which applicant relies (i.e., that the via holes of the interposer or second layer are ***plated through holes)*** are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. The claim recites that the second substrate or power layer is: "laminated to said first substrate and having conductive, adhesive-filled via through holes that align with, and make electrical contact with, the conductive via through holes of said first substrate". DiStefano clearly teaches that the interposer or second layer (second substrate from the top of Figure 2) is laminated to said first substrate (as seen in Figure 3) and having conductive, adhesive-filled via through holes (the holes that are filled with Reference number 48) that align with (as clearly seen in Figure 3), and make

electrical contact with, the conductive via through holes (reference number 26) of said first substrate (top substrate of Figure 2).

Appellant further argues, on page 5 of the Appeal Brief, that: *"one merely has to read further and observe the amorphous, flowable structure of the interposer layer shown in figure 3,4,5,etc., to realize the non-alignment of the hole (via) of the second, or interposer layer with the plated vias of either the first or third layers" and that "the hole structures....are not distinctly described as aligned by DiStefano et al, but merely matched"*. However, the examiner respectfully disagrees with this argument. DiStefano specifically teaches that the invention: "preferably includes the step of stacking the circuit panels and interposers in superposed relation so that each interposer is disposed between two circuit panels, with the major surfaces of the interposers and circuit panels confronting one another, and with interconnect locations on the confronting surfaces of the circuit panels and interposers being **aligned** with one another" (column 5, lines 10-18). Therefore, we can conclude that the plated vias of the first and third layers are indeed **aligned** with the via of the second or interposer layer.

Appellant further argues, on page 6 of the Appeal Brief, that: "claim 5 describes holes, whose conductive pads are slightly undercut" and that: " There is simply no such recitation in the text of DiStefano et al. In response to applicant's argument, it is noted that the features upon which applicant relies (i.e., that the conductive pads are slightly undercut) are not recited in rejected claim 5. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. Furthermore, assuming appellant erroneously referred to claim 5 instead of claim 4,

which discloses the limitation that: "said via through holes of said power core layer comprise undercut contact surfaces", it is noted that as stated in the rejection: "DiStefano teaches that said via through holes (the holes where reference number 48 is located) of said inner power core layer comprise undercut contact surfaces (the top and bottom surfaces of the conductive material reference number 48 inside the via through hole, as seen in Figure 3). Therefore, we can conclude that DiStefano teaches that said via through holes of said inner power core layer comprise undercut contact surfaces.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

KAMMIE CUNEO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

Appeal Conference Conferees:

José H. Alcalá

Examiner – Art Unit 2827

Kammie Cuneo

SPE – Art Unit 2829

Olik Chaudhuri OC

SPE – Art Unit 2823

September 6, 2003

Mark Levy
Salzman & Levy
19 Chenango St.,Ste.902
Binghamton, NY 13901